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10/759,570	01/20/2004	Takahiko Murata	60188-754	8016
7590 09/04/2008 Jack Q. Lever, Jr. McDERMOTT, WILL & EMERY 600 Thirteenth Street, N.W. Washington, DC 20005-3096				
EXAMINER CUTLER, ALBERT H				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/759,570

Applicant(s)

MURATA ET AL.

Examiner

ALBERT H. CUTLER

Art Unit

2622

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 May 2008.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 4.5.12 and 14-24 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 4.5.12 and 14-24 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/S508)
Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____

DETAILED ACTION

1. This office action is responsive to communication filed on May 29, 2008.

Response to Arguments

2. Applicant's arguments filed May 29, 2008 with respect to claims 4 and 12 have been fully considered but they are not persuasive.
3. Applicant argues that Watanabe fails to describe or suggest a solid state imaging apparatus including, among other features, a signal output circuit configured to perform one of two types of operations, wherein the signal output circuit includes: a first shift register for sequentially outputting selection signals, which select each pixel, to **all** of the plurality of the pixels either in a vertical or a horizontal direction and a second shift register for continuously outputting the selection signals to some of the plurality of pixels having color filters of the same color either in a vertical or a horizontal direction partially. Applicant further asserts that all pixel signals in a horizontal direction are not output unless both of the alleged first shift register 12 and the alleged second shift register 13 are operated.
4. The Examiner respectfully disagrees. First, it is assumed that Applicant is referring to Moraillon, and not Watanabe, as Watanabe is not cited in the current rejection. The Examiner agrees with Applicant's assertion that all pixel signals in a horizontal direction are not output unless **both** shift registers are operated. However, claim 4 recites, "a first shift register for sequentially outputting selection signals, which select each pixel, to **all** of the plurality of the pixels **either** in a vertical or a horizontal direction". The first shift register (12) of Moraillon selects all of the plurality of pixels in

the vertical direction (i.e. selects all of the green pixels), column 2, line 54 through column 3, line 7, figure 3. As the first shift register (12) does not skip any of the pixels in the vertical direction, it satisfies the limitation of outputting selection signals to all of the plurality of the pixels in the vertical direction. The fact that the first shift register (12) may not select all of the pixels in the horizontal direction is moot, as claims 4 and 12 call for the selection of all pixels in **either** the vertical or horizontal directions.

5. Therefore, the rejection of claims 4, 12, 14, 16, 17 and 20 is maintained by the Examiner.

6. Applicant's arguments with respect to claims 5, 15, 18, 19 and 21 have been fully considered but they are not persuasive.

7. Consider claim 5. Applicant argues that due to the thinning-out operation of Terada et al., some (not all) pixels having color filters of the same color are sequentially output by the mode selection means.

8. The Examiner respectfully disagrees. Claim 5 recites that selection signals are continuously output to all pixels having color filters of the same color either in the vertical or the horizontal direction "partially". Terada et al. teaches in column 26, line 41 through column 28, line 31 that selection signals are continuously output to pixels having the same color in the vertical direction and the horizontal directions. As selection signals are sequentially sent to groups of pixels having the same color, the selection signals are sent to all pixels having a green color (i.e. "all" the selected pixels are green), and then sent to all pixels having a red color (i.e. "all" the selected pixels are red), and finally to all pixels having a blue color (i.e. "all" the selected pixels are blue).

Furthermore, claim 5 calls for the selection signals to be output to pixels in the vertical or horizontal direction "partially". As only some of the pixels are output by Terada et al., as asserted by Applicant, pixels are partially selected in the vertical and horizontal direction.

9. Therefore, the rejection of claims 5, 15, 18, 19 and 21 is maintained by the Examiner.

Claim Rejections - 35 USC § 102

10. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

11. Claims 4, 12, 14 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Moraillon 4,553,159).

Consider **claim 4**, Moraillon teaches:

A solid state imaging apparatus (figure 3), comprising:

a plurality of pixels two-dimensionally arranged in a vertical direction and a horizontal direction (see figures 2 and 3) wherein each of the plurality of pixels has a color filter having a different color from color filters of vertically **or horizontally** adjacent pixels (Each of the plurality of pixels has a color filter having a different color from color filters of horizontally adjacent pixels. See figures 2 and 3, column 2, lines 23-36); and

a signal output circuit(12, 13, 14, 15) configured to perform one of two types of operations(The signal output circuit performs operations for outputting the green pixels alone and for outputting the red and blue pixels, column 2, line 42 through column 3, line 7), wherein the signal output circuit includes:

a first shift register(12, figure 3) for sequentially outputting selection signals, which select each pixel, to all of the plurality of the pixels either in a **vertical** or a horizontal direction(The first shift register(12) selects all the plurality of pixels in vertical direction(i.e. selects all the green pixels). See column 2, line 54 through column 3, line 7, figure 3.), and

a second shift register(13) for continuously outputting the selection signals to some of the plurality of pixels having color filters of the same color either in a vertical or a **horizontal direction partially**(The second shift register continuously selects pixels having red color filters in the horizontal direction, and then continuously selects pixels having blue color filters in the horizontal direction, column 2, line 42 through column 3, line 7.).

The first shift register (12) of Moraillon selects all of the plurality of pixels in the vertical direction (i.e. selects all of the green pixels), column 2, line 54 through column 3, line 7, figure 3. As the first shift register (12) does not skip any of the pixels in the vertical direction, it satisfies the limitation of outputting selection signals to all of the plurality of the pixels in the vertical direction. The fact that the first shift register (12) may not select all of the pixels in the horizontal direction is moot, as claims 4 and 12 call for the selection of all pixels in **either** the vertical or horizontal directions.

Consider **claim 12**, Moraillon teaches:

A camera(column 1, lines 7-8, column 2, lines 10-36) comprising a solid state imaging apparatus(figure 3), comprising:

a plurality of pixels two-dimensionally arranged in a vertical direction and a horizontal direction(see figures 2 and 3) wherein each of the plurality of pixels has a color filter having a different color from color filters of vertically **or horizontally** adjacent pixels(Each of the plurality of pixels has a color filter having a different color from color filters of horizontally adjacent pixels. See figures 2 and 3, column 2, lines 23-36); and

a signal output circuit(12, 13, 14, 15) configured to perform one of two types of operations(The signal output circuit performs operations for outputting the green pixels alone and for outputting the red and blue pixels, column 2, line 42 through column 3, line 7), wherein the signal output circuit includes:

a first shift register(12, figure 3) for sequentially outputting selection signals, which select each pixel, to all of the plurality of the pixels either in a **vertical** or a horizontal direction(The first shift register(12) selects all the plurality of pixels in vertical direction(i.e. selects all the green pixels). See column 2, line 54 through column 3, line 7, figure 3.), and

a second shift register(13) for continuously outputting the selection signals to some of the plurality of pixels having color filters of the same color either in a vertical or a **horizontal direction partially**(The second shift register continuously selects pixels having red color filters in the horizontal direction, and then continuously selects pixels

having blue color filters in the horizontal direction, column 2, line 42 through column 3, line 7.).

12. The first shift register (12) of Moraillon selects all of the plurality of pixels in the vertical direction (i.e. selects all of the green pixels), column 2, line 54 through column 3, line 7, figure 3. As the first shift register (12) does not skip any of the pixels in the vertical direction, it satisfies the limitation of outputting selection signals to all of the plurality of the pixels in the vertical direction. The fact that the first shift register (12) may not select all of the pixels in the horizontal direction is moot, as claims 4 and 12 call for the selection of all pixels in **either** the vertical or horizontal directions.

Consider **claim 14**, and as applied to claim 4 above, Moraillon further teaches:
the second shift register(13) repeats, after continuously outputting signals of the plurality of pixels having color filters of the same color(red), an operation which continuously outputs signals of the plurality of pixels having color filters of a different color(blue), on a basis of each pixel mixture unit consisting of a plurality of pixels(See figure 3, column 2, line 49 through column 3, line 7.), and the pixel mixture unit consists of 25 pixels arranged in five rows and five columns(See figure 3, the pixel mixture unit(i.e. those pixels read out to the second shift register(13)) consists of five columns and five or more rows.).

Consider **claim 16**, and as applied to claim 4 above, Moraillon further teaches:

the first shift register(12) performs a regular operation(The first shift register only shifts out pixels of a single color.), and a second shift register(13) performs a pixel mixture operation(The second shift register shifts out a mixture of red and blue pixels. See column 2, line 42 through column 3, line 7.).

13. Claims 5, 15, 18, 19 and 21, 23 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Terada et al.(US 6,124,888).

Consider claim 5, Terada et al. teach:

A solid state imaging apparatus(figure 25-29B), comprising:

a plurality of pixels(608) two-dimensionally arranged in a vertical direction and a horizontal direction(see figure 26, 27A, 27B) wherein each of the plurality of pixels has a color filter having a different color from color filters of vertically or horizontally adjacent pixels(see figure 27A); and

a signal output circuit(figures 25 and 26) configured to perform one of two types of operations(Still image operations and video operations are performed, column 25, lines 37-63.), wherein the signal output circuit includes:

a shift register(610) for sequentially outputting via a selector switch selection signals, which select each pixel(Switches SW1, SW2, etc. are used to select each pixel, column 26, lines 5-22. These switches are comprised of transistors, see 3, figure 1, column 7, lines 4-26.), to all of the plurality of pixels either in a vertical or a horizontal

direction(Selection signals are sent to all pixels in a still image mode, column 25, lines 46-54.) and

an operation switching circuit(Mode selection means, 607, Switches SW1, SW2, etc.) for outputting the selection signals from the shift register(column 25, lines 37-63, column 26, lines 5-22), the operation switching circuit configured to switch between a first signal transmission method in which the selection signals are sequentially output to all pixels either in the vertical direction or the horizontal direction(Selection signals are sent to all pixels in a still image mode, column 25, lines 46-54.) and a second signal transmission method in which the selection signals are continuously output to all pixels having color filters of the same color either in the vertical direction or the horizontal direction partially(In the video mode, selection signals are continuously output to pixels having the same color in vertical direction and the horizontal direction, figure 27A, column 26, line 41 through column 28, line 31. As selection signals are sequentially sent to groups of pixels having the same color, the selection signals are sent to all pixels having a green color (i.e. "all" the selected pixels are green), and then sent to all pixels having a red color (i.e. "all" the selected pixels are red), and finally to all pixels having a blue color (i.e. "all" the selected pixels are blue). Furthermore, as only some of the pixels are output by Terada et al., pixels are "partially" selected in the vertical and horizontal direction.).

Consider claim 15, and as applied to claim 5 above, Terada et al. further teach:

the second signal transmission method repeats, after continuously outputting signals of the plurality of pixels having color filters of the same color(for example, green), an operation which continuously outputs signals of the plurality of pixels having color filters of a different color(for example, red, column 26, line 63 through column 27, line 14), on a basis of each pixel mixture unit consisting of a plurality of pixels(four pixels are mixed(i.e. added together), column 28, lines 17-27, figure 27A), and

the pixel mixture unit consists of 25 pixels arranged in five rows and five columns(Terada et al. teach that the number of pixels to be added is not limited to four, column 28, lines 21-22.).

Consider claim 18, and as applied to claim 5 above, Terada et al. further teach:

the first signal transmission method is a sequential scanning method, and the second transmission method is a pixel mixture scanning method(In the first method, all pixels are read out, whereas, in the second method, the pixels are thinned and groups of four same-colored pixels are mixed, column 25, lines 36-63, column 28, lines 17-27.).

Consider claim 19, and as applied to claim 18 above, Terada et al. further teach:

a static image mode is executed by the sequential scanning method, and a moving image mode is executed by the pixel mixture scanning method(column 25, lines 37-63).

Consider claim 21, and as applied to claim 5 above, Terada et al. further teach the solid state imaging apparatus is of a MOS type, and the operation switching circuit comprises a plurality of MOS transistors selected by a plurality of gate signal lines(column 9, lines 18-39).

Consider claim 23, and as applied to claim 5 above, Terada et al. further teaches that the first signal transmission method sequentially outputs all the pixel signals having color filters of the different colors from one another (See column 25, lines 46-54. The pixels are read out without thinning in the still image mode. As the pixels are not thinned, all pixel signals having color filters of the different colors from one another are output.).

Consider claim 24, and as applied to claim 5 above, Terada et al. further teaches that the selector switch comprises a transistor(Switches SW1, SW2, etc. are used to select each pixel, column 26, lines 5-22. These switches are comprised of transistors, see 3, figure 1, column 7, lines 4-26.).

Claim Rejections - 35 USC § 103

14. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
15. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moraillon(US 4,553,159).

Consider claim 17, and as applied to claim 16 above, Moraillon teaches of a camera(column 1, lines 7-8, column 2, lines 10-36) which performs a regular operation and a pixel mixture operation(see claim 16 rationale) using a solid state imaging array(column 1, lines 10-15, column 2, lines 10-36). Moraillon teach that both the regular operation and the pixel mixture operation are performed every time the imager is read out, regardless of what kind of imaging mode the camera might be in(column 2, line 42 through column 3, line 7). However, Moraillon does not explicitly teach that a static image mode is executed by the regular operation, and a moving image mode is executed by the pixel mixture operation.

However, Official Notice (MPEP § 2144.03) is taken that both the concepts and advantages of using a solid state imaging array in both a static mode and a moving image mode are well known and expected in the art. It would have been obvious to a person having ordinary skill in the art at the time of the invention to include both static image and moving image modes in the camera taught by Moraillon for the benefit of increasing the versatility and marketability of the camera.

It should be noted that the common knowledge for using a solid state imaging array in both a static mode and a moving image mode **is taken as admitted prior art** because Applicant failed to seasonably traverse this common knowledge from the amendment filed on May 29, 2008. See MPEP § 2144.03. In re Chevenard, 60 USPQ 239 (CCPA 1943).

16. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moraillon in view of Skow et al.(US 2004/0085475).

Consider claim 20, and as applied to claim 4 above, Moraillon further teaches that the first and second shift registers(12 and 13) are laid out in the same direction(see figure 3).

However, Moraillon does not explicitly teach that the solid state imaging apparatus is of a MOS type.

Skow et al. are similar to Moraillon in that Skow et al. teach of a camera(figure 1, paragraph 0024) including an imaging array comprising pixels covered with red, green and blue color filters(see figure 5, paragraph 0058).

However, in addition to the teachings of Moraillon, Skow et al. teach that the solid state imaging apparatus is of a MOS type(paragraph 0025).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to embody the imaging apparatus taught by Moraillon using MOS technology as taught by Skow et al. for the benefit that MOS devices have high speed and extremely low power consumption(Skow et al., paragraph 0025).

17. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moraillon in view of Parulski et al. (US 5,440,343).

Consider claim 22, and as applied to claim 4 above, Moraillon does not explicitly teach that the first shift register outputs all the pixel signals having color filters of the different colors from one another.

Parulski et al. similarly teaches a solid state imaging apparatus (see figures 4 and 9), comprising a plurality of pixels two-dimensionally arranged in a vertical direction and a horizontal direction wherein each of the plurality of pixels has a color filter having a different color from color filters of vertically or horizontally adjacent pixels (see 40, figure 4), and a signal output circuit (see 48 and 49, figure 9) configured to perform one of two types of operations, wherein the signal output circuit (48 and 49) includes a first shift register for sequentially outputting selection signals, which select each pixel, to all of the plurality of the pixels either in a vertical or a horizontal direction (The horizontal output register (48) outputs all of the plurality of pixels when in a still image mode of operation, column 5, lines 22-25.) and a second shift register (49) for continuously outputting the selection signals to some of the plurality of pixels having color filters of the same color either in a vertical or a horizontal direction partially (Each shift register (48, 49) comprises two registers (50, 52) as shown in figure 4. The top register (50) outputs some of the plurality of pixels having color filters of the same color (i.e. green), column 4, lines 65-69. The green pixels are partially output via register 49 of figure 9 as the first and last 128 pixels in the horizontal direction are not output, column 7, lines 37-46.).

However, in addition to the teachings of Moraillon, Parulski et al. teaches that the first shift register (48) outputs all the pixel signals having color filters of the different

colors from one another (All 1536 pixels in the horizontal direction are output via the first shift register (48), column 7, lines 1-46.).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to configure the shift registers of Moraillon in the manner taught by Parulski et al. such that the first shift register outputs all pixel signals having color filters of the different colors from one another for the benefit of enabling the output of different aspect ratio images (Parulski et al., column 7, lines 1-12) and thus creating a more versatile and valuable device.

Conclusion

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALBERT H. CUTLER whose telephone number is (571)270-1460. The examiner can normally be reached on Mon-Thu (9:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc-Yen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/AC/
08/27/2008

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Supervisory Patent Examiner, Art Unit 2622***